REMARKS

This is intended as a full and complete response to the Office Action dated May 4, 2006, having a shortened statutory period for response set to expire on August 4, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 1-22 remain pending following entry of this response. Claim 16 has been amended. Applicants submit that the amendment does not introduce new matter.

Claim Rejections - 35 U.S.C. § 102

Claims 1-8 and 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by *Haupt* (US Patent No. 6,334,159).

Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Haupt* does not disclose “each and every element as set forth in the claim.” For example, *Haupt* does not disclose the claim 1, 16 and 22 limitation of “a transfer bus for communication between the memory control device and the memory modules, wherein the transfer bus is in the form of a concatenated bus structure.” Concatenated is commonly defined as “connected or linked in a series.” (See http://dictionary.reference.com/browse/concatenated). Therefore, a concatenated bus structure is one which connects devices to the bus in a series. As Applicants point out

in greater detail below, *Haupt* does not disclose a bus structure where devices are connected in series and thus does not disclose a concatenated bus structure.

Haupt is directed to a method and an apparatus for scheduling requests within a data processing system. (*Haupt*, Title) The apparatus of *Haupt* contains a plurality of processing modules 120A each connected to a plurality of memory storage units 110A-D. (See *Haupt*, Figure 2).

The Examiner argues that *Haupt* discloses a concatenated bus structure at Column 5, Lines 40-51. However, the text cited by the Examiner does not describe a concatenated bus structure, rather the cited text describes the functionality of a memory controller.

Furthermore, in contrast to a concatenated bus structure, there are no connections between memory storage units in *Haupt*. (*Haupt*, Figure 2). In contrast, the only connections to memory storage units in *Haupt* are between the processing modules and the memory storage units. (*Haupt*, Column 4, Lines: 64-66). *Haupt* illustrates the interfaces between the processing modules and the memory storage units in Figure 1 as being solely between processing modules and memory storage units. (*Haupt*, Figure 1). Thus, in *Haupt* the processing modules are connected in parallel to the memory storage units. Consequently, *Haupt* does not disclose a concatenated bus structure, rather *Haupt* describes a parallel bus structure.

Therefore, claims 1, 16 and 22 are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Haupt* (US Patent No 6,334,159). The Examiner takes Official Notice that "it would have been obvious to a person of ordinary skill in the art to include an on-die termination signal in the memory system of *Haupt*." Applicants respectfully traverse this rejection.

With regards to Official Notice, section 2144.03(A) of the MPEP states "assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art." Applicants note that contrary to MPEP section 2144.03, no evidentiary support of the Examiner's obviousness conclusion has been cited in the Office Action. Consequently, Applicants respectfully request evidentiary support of the Examiner's conclusion that it would have been obvious "to include an on-die termination signal in the memory system of *Haupt*."

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Gero G. McClellan, Reg. No. 44,227/
Gero G. McClellan
Registration No. 44,227
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants